

CD74HC192, CD74HC193, CD74HCT193

High Speed CMOS Logic Presettable Synchronous 4-Bit Up/Down Counters

Features

- Synchronous Counting and Asynchronous Loading
- Two Outputs for N-Bit Cascading
- Look-Ahead Carry for High-Speed Counting
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

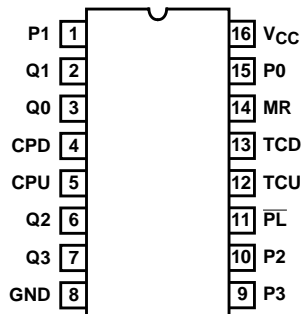
The Harris CD74HC192, CD74HC193 and CD74HCT193 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

Presetting the counter to the number on the preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input (\overline{PL}). The counter is incremented on the low-to-high transition of the Clock-Up input (and a high level on the Clock-Down input) and decremented on the low to high transition of the Clock-Down input (and a high level on the Clock-up input). A high level on the MR input overrides any other input to clear the counter to its zero state. The Terminal Count up (carry) goes low half a clock period before the zero count is reached and returns to a high level at the zero count. The Terminal Count Down (borrow) in the count down mode likewise goes low half a clock period before the maximum count (9 in the 192 and 15 in the 193) and returns to high at the maximum count. Cascading is effected by connecting the carry and borrow outputs of a less significant counter to the Clock-Up and CLock-Down inputs, respectively, of the next most significant counter.

If a decade counter is present to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

Pinout

CD74HC192, CD74HC193, CD74HCT193
(PDIP, SOIC)
TOP VIEW



Ordering Information

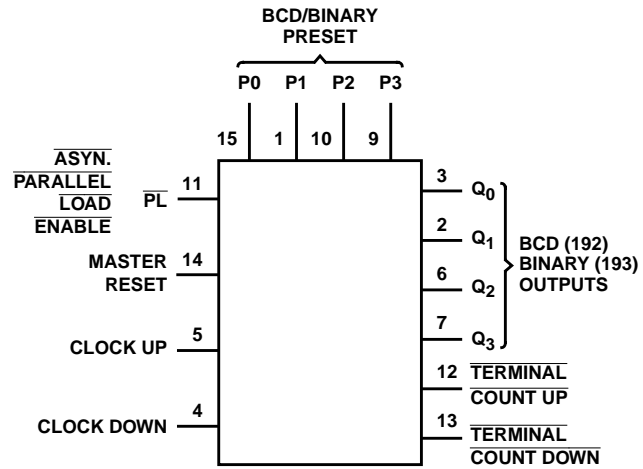
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC192E	-55 to 125	16 Ld PDIP	E16.3
CD74HC193E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT193E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT193M	-55 to 125	16 Ld SOIC	M16.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

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Functional Diagram



TRUTH TABLE

CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD	FUNCTION
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset Inputs

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level

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Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC} or I_{GND}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^{\circ}C/W$)
PDIP Package	90
SOIC Package	160
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range (T_A)	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types	.2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS		
		V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX			
HC TYPES														
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V		
				4.5	3.15	-	-	3.15	-	3.15	-	V		
				6	4.2	-	-	4.2	-	4.2	-	V		
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V		
				4.5	-	-	1.35	-	1.35	-	1.35	V		
				6	-	-	1.8	-	1.8	-	1.8	V		
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V		
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V		
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V		
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V		
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V		
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V		
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V		
			0.02	6	-	-	0.1	-	0.1	-	0.1	V		
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V		
			5.2	6	-	-	0.26	-	0.33	-	0.4	V		
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA		
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μA		

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DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	-	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} to GND	-	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	-	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
P0-P3	0.4
MR	1.45
PL	0.85
CPU, CPD	1.45

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360μA max at 25°C.

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Prerequisite For Switching Specifications

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
Pulse Width CPU, CPD 192	t _W	2	115	-	-	145	-	175	-	ns
		4.5	23	-	-	29	-	35	-	ns
		6	20	-	-	25	-	30	-	ns
CPU, CPD 193	t _W	2	100	-	-	125	-	150	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	17	-	-	21	-	26	-	ns
$\overline{\text{PL}}$	t _W	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
MR	t _W	2	100	-	-	125	-	150	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	17	-	-	21	-	26	-	ns
Set-up Time P _n to $\overline{\text{PL}}$	t _{SU}	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Hold Time P _n to $\overline{\text{PL}}$	t _H	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
Hold Time CPD to CPU or CPU to CPD	t _H	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Recovery Time $\overline{\text{PL}}$ to CPU, CPD	t _{REC}	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
MR to CPU, CPD	t _{REC}	2	5	-	-	5	-	5	-	ns
		4.5	5	-	-	5	-	5	-	ns
		6	5	-	-	5	-	5	-	ns
Maximum Frequency CPU, CPD 192	f _{MAX}	2	5	-	-	4	-	3	-	MHz
		4.5	22	-	-	18	-	15	-	MHz
		6	24	-	-	21	-	18	-	MHz
CPU, CPD 193	f _{MAX}	2	5	-	-	4	-	3	-	MHz
		4.5	25	-	-	20	-	17	-	MHz
		6	29	-	-	24	-	20	-	MHz
HCT TYPES										
Pulse Width CPU, CPD 192	t _W	2	-	-	-	-	-	-	-	ns
		4.5	23	-	-	29	-	35	-	ns
		6	-	-	-	-	-	-	-	ns
CPU, CPD 193	t _W	2	-	-	-	-	-	-	-	ns
		4.5	23	-	-	29	-	35	-	ns
		6	-	-	-	-	-	-	-	ns

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Prerequisite For Switching Specifications (Continued)

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
\overline{PL}	t_W	2	-	-	-	-	-	-	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	-	-	-	-	-	-	-	ns
MR	t_W	2	-	-	-	-	-	-	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	-	-	-	-	-	-	-	ns
Set-up Time P _n to \overline{PL}	t_{SU}	2	-	-	-	-	-	-	-	ns
		4.5	15	-	-	19	-	22	-	ns
		6	-	-	-	-	-	-	-	ns
Hold Time P _n to \overline{PL}	t_H	2	-	-	-	-	-	-	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	-	-	-	-	-	-	-	ns
Hold Time CPD to CPU or CPU to CPD	t_H	2	-	-	-	-	-	-	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	-	-	-	-	-	-	-	ns
Recovery Time \overline{PL} to CPU, CPD	t_{REC}	2	-	-	-	-	-	-	-	ns
		4.5	15	-	-	19	-	22	-	ns
		6	-	-	-	-	-	-	-	ns
MR to CPU, CPD	t_{REC}	2	-	-	-	-	-	-	-	ns
		4.5	5	-	-	5	-	5	-	ns
		6	-	-	-	-	-	-	-	ns
Maximum Frequency CPU, CPD 192	f_{MAX}	2	-	-	-	-	-	-	-	MHz
		4.5	22	-	-	18	-	15	-	MHz
		6	-	-	-	-	-	-	-	MHz
CPU, CPD 193	f_{MAX}	2	-	-	-	-	-	-	-	MHz
		4.5	22	-	-	18	-	15	-	MHz
		6	-	-	-	-	-	-	-	MHz

Switching Specifications Input $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay CPU to $\overline{\text{TCU}}$	$t_{\text{PLH}}, t_{\text{PHL}}$	C _L = 50pF	2	-	-	125	-	155	-	190	ns
		C _L = 50pF	4.5	-	-	25	-	31	-	38	ns
		C _L = 15pF	5	-	10	-	-	-	-	-	ns
		C _L = 50pF	6	-		21	-	26	-	32	ns
CPD to $\overline{\text{TCD}}$	$t_{\text{PLH}}, t_{\text{PHL}}$	C _L = 50pF	2	-	-	125	-	155	-	190	ns
		C _L = 50pF	4.5	-	-	25	-	31	-	38	ns
		C _L = 15pF	5	-	10	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	21	-	26	-	32	ns
CPU to Q _n	$t_{\text{PLH}}, t_{\text{PHL}}$	C _L = 50pF	2	-	-	220	-	270	-	325	ns
		C _L = 50pF	4.5	-	-	43	-	54	-	65	ns
		C _L = 15pF	5	-	18	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	37	-	46	-	55	ns

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Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CPD to Q_n	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	220	-	270	-	325	ns
		$C_L = 50\text{pF}$	4.5	-	-	43	-	54	-	65	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	37	-	46	-	55	ns
\overline{PL} to Q_n	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	220	-	275	-	330	ns
		$C_L = 50\text{pF}$	4.5	-	-	44	-	55	-	66	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	37	-	47	-	56	ns
MR to Q_n	t_{PHL}	$C_L = 50\text{pF}$	2	-	-	200	-	250	-	300	ns
		$C_L = 50\text{pF}$	4.5	-	-	40	-	50	-	60	ns
		$C_L = 15\text{pF}$	5	-	17	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	34	-	43	-	51	ns
Transition Time Q, TCU, TCD	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}	$C_L = 15\text{pF}$	5	-	40	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay CPU to \overline{TCU}	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	27	-	34	-	41	ns
		$C_L = 15\text{pF}$	5	-	11	-	-	-	-	-	ns
CPU to \overline{TCD}	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	27	-	34	-	41	ns
		$C_L = 15\text{pF}$	5	-	11	-	-	-	-	-	ns
CPU to Q_n	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	40	-	50	-	60	ns
		$C_L = 15\text{pF}$	5	-	17	-	-	-	-	-	ns
CPD to Q_n	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	40	-	50	-	60	ns
		$C_L = 15\text{pF}$	5	-	17	-	-	-	-	-	ns
\overline{PL} to Q_n	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	46	-	58	-	69	ns
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
MR to Q_n	t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	43	-	54	-	65	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
Transition Time Q, TCU, TCD	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$									
			4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_{IN}	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}	$C_L = 15\text{pF}$	5	-	50	-	-	-	-	-	pF

NOTES:

5. C_{PD} is used to determine the dynamic power consumption, per gate.
6. $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

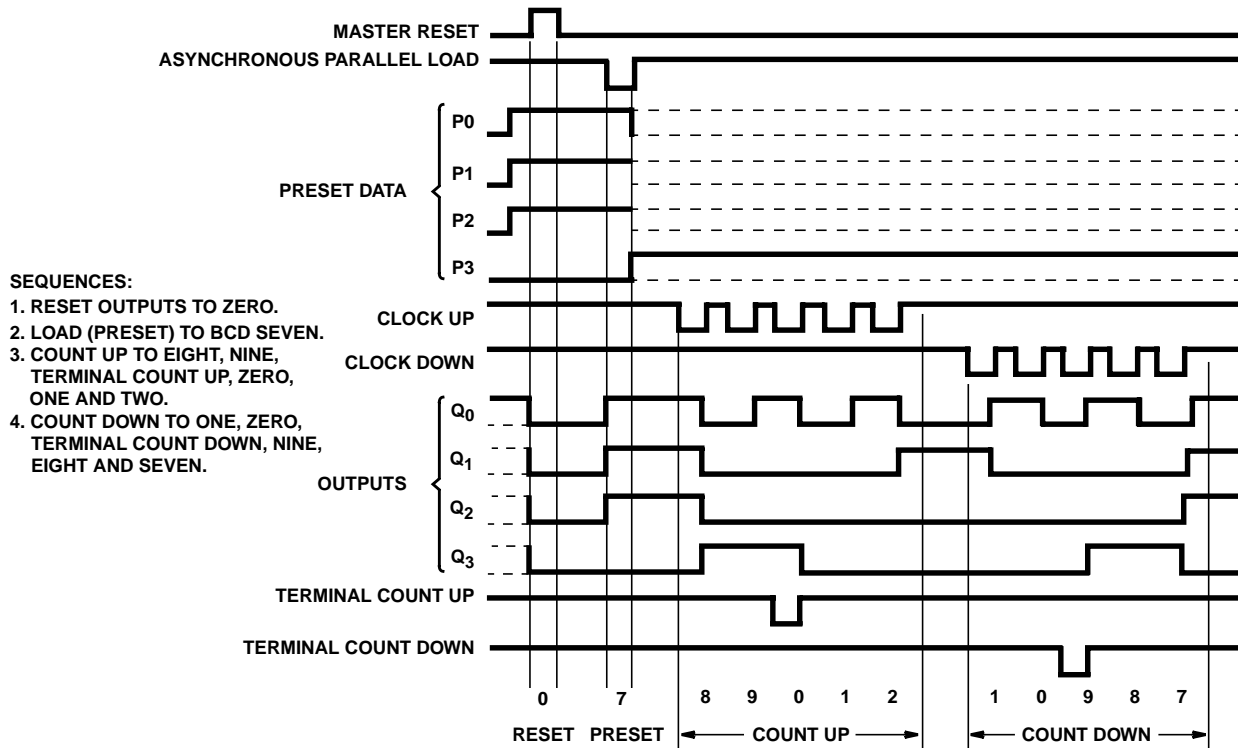


FIGURE 1. CD74HC192 SYNCHRONOUS DECADE COUNTERS, TYPICAL RESET, PRESET AND COUNT SEQUENCES

Test Circuits and Waveforms (Continued)

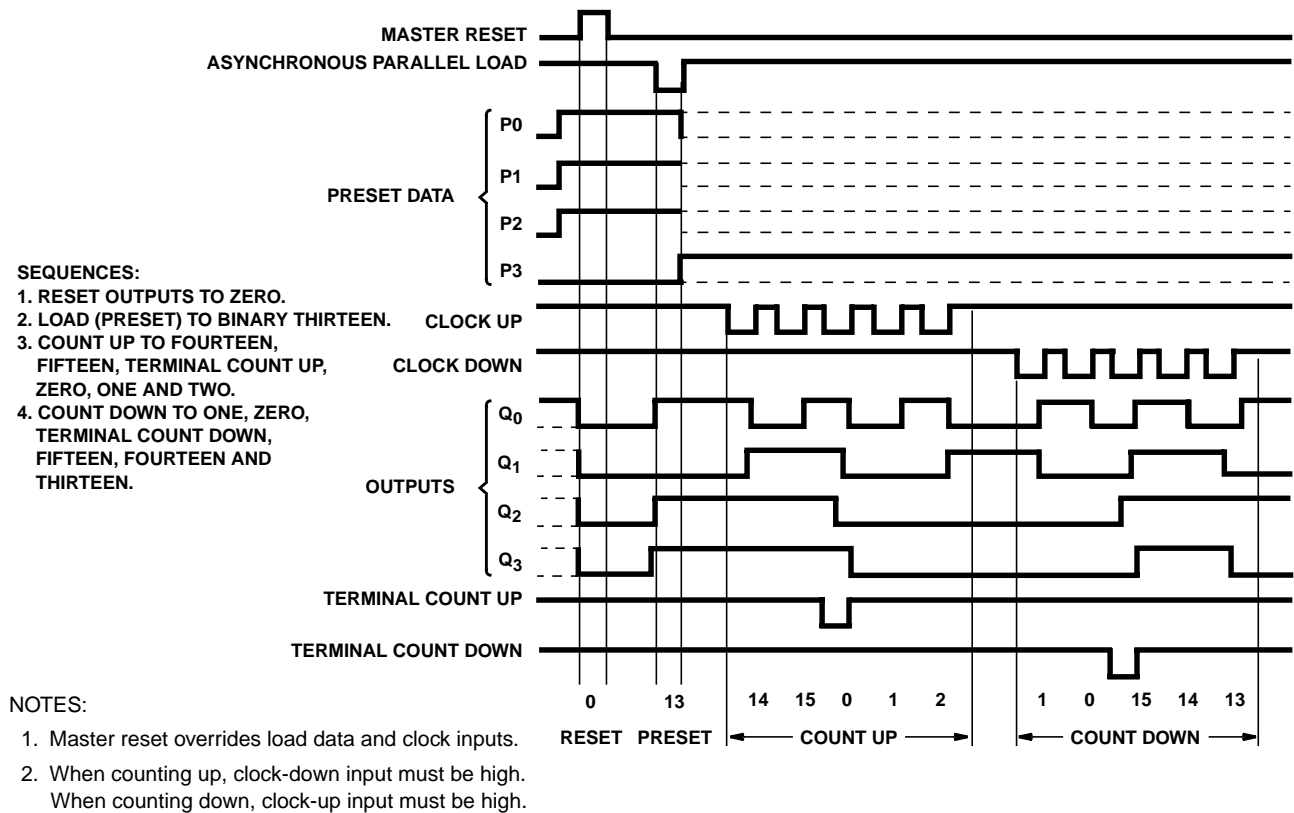


FIGURE 2. CD74HC193 SYNCHRONOUS BINARY COUNTERS, TYPICAL RESET, PRESET AND COUNT SEQUENCES

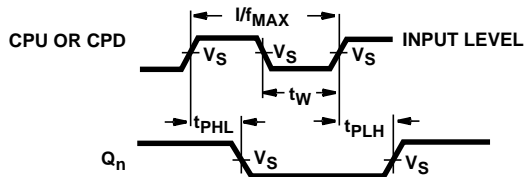


FIGURE 3. CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH

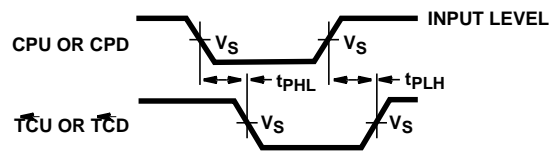


FIGURE 4. CLOCK TO TERMINAL COUNT DELAYS

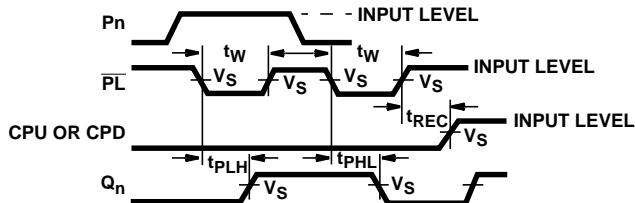


FIGURE 5. PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAYS, AND PARALLEL LOAD TO CLOCK RECOVERY TIME

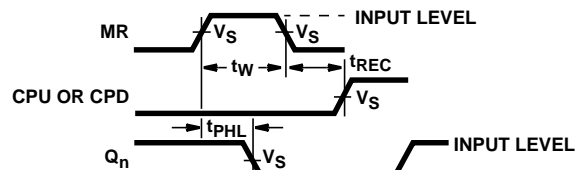


FIGURE 6. MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



FIGURE 9. CD74HC192, CD74HCT193 STATE DIAGRAMS

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